What is claimed is:

1. A semiconductor memory comprising a memory cell matrix including a plurality of cell columns arranged along a row-direction, each of cell columns is implemented by a plurality of memory cell transistors serially arranged along a column-direction, the memory cell matrix comprising:

a plurality of device isolation films running along the column-direction, arranged alternatively between the cell columns;

a plurality of first conductive layers having top surfaces lower than the level of top surfaces of the device isolation films, arranged along the row and column-directions, a group of the first conductive layers arranged along the column-direction is assigned to a corresponding cell column, adjacent groups of the first conductive layers assigned to adjacent cell columns are isolated from each other by the device isolation film disposed between the adjacent groups;

a plurality of inter-electrode dielectrics arranged selectively and respectively on the corresponding first conductive layers, the inter-electrode dielectric has a dielectric constant larger than that of silicon oxide; and

a plurality of second conductive layers running along the row-direction, each of the second conductive layers

arranged on the inter-electrode dielectric and the device isolation films so that the second conductive layer can be shared by the memory cell transistors arranged along the row-direction belonging to different cell columns.

2. The semiconductor memory of claim 1, wherein each of the inter-electrode dielectrics is embedded at least a portion of a space defined by the top surface corresponding to a level of the top surfaces of the device isolation films and the bottom surface corresponding to a level of the top surfaces of the first conductive layers.

3. The semiconductor memory of claim 2, wherein a thickness of the inter-electrode dielectrics is thinner than the difference between the level of the top surfaces of the device isolation films and the level of the top surfaces of the first conductive layers, and each of the bottom surfaces of the inter-electrode dielectrics contacts with side surfaces of the device isolation films and the top surface of the corresponding first conductive layer.

4. The semiconductor memory of claim 3, further comprising auxiliary conductive layers filled respectively in isolated spaces, each of which are defined by the bottom surface of the

corresponding second conductive layer and the top surface of the corresponding inter-electrode dielectric.

5. The semiconductor memory of claim 3, wherein the thickness of each of the inter-electrode dielectrics at both edges near the device isolation film is thicker than that at central portion.

6. The semiconductor memory of claim 3, wherein each of the top surfaces of the first conductive layers manifests a curved surface such that both edges of the curved surface are higher than the level of the central portion of the curved surface.

7. The semiconductor memory of claim 2, wherein the space, in which the inter-electrode dielectrics is embedded, manifests a topology of a rectangular groove, whose sidewalls encroach laterally corresponding side walls of adjacent device isolation films so as to widen the width of the rectangular groove.

8. The semiconductor memory of claim 1, wherein each of the inter-electrode dielectrics is a single layer film selected from the group consisting of an silicon oxide film, a silicon nitride film, an aluminum oxide film, a hafnium oxide film and a zirconium

oxide film or a composite film including at least one of the single layer film.

9. A method for manufacturing a semiconductor memory comprising a memory cell matrix including a plurality of cell columns arranged along a row-direction, each of cell columns is implemented by a plurality of memory cell transistors serially arranged along a column-direction, the method comprising:

forming a periodic structure implemented by first and second ridges, both running alternately along the column-direction, each of the first ridges is made of device isolation film and each of the second ridges is made of one of protruding portions of a semiconductor substrate, a cell site gate insulator on the protruding portion of the semiconductor substrate and a first conductive layer on the cell site gate insulator, the top surface of the second ridges is lower than the top surface of the first ridges, each of the second ridges is assigned to a corresponding cell column;

forming a plurality of inter-electrode dielectrics on the corresponding first conductive layers such that adjacent inter-electrode dielectrics are isolated by one of the first ridges, the inter-electrode dielectric has a dielectric constant larger than that of silicon oxide; and

forming a plurality of second conductive layers running along the row-direction, each of the second conductive layers

arranged on the inter-electrode dielectric and the device isolation films so that the second conductive layer can be shared by the memory cell transistors arranged along the row-direction belonging to different cell columns.

10. The method of claim 9, wherein the forming inter-electrode dielectrics comprises:

blanket forming the inter-electrode dielectric so as to cover the top surfaces of the first conductive layers, the top surfaces of the device isolation films and steps defined by the top surfaces of the first and second ridges; and

planarizing the top surface of the inter-electrode dielectric so as to expose the top surfaces of the device isolation films.

11. The method of claim 9, wherein the forming inter-electrode dielectrics comprises:

blanket forming the inter-electrode dielectric so as to cover the top surfaces of the first conductive layers, the top surfaces of the device isolation films and steps defined by the top surfaces of the first and second ridges;

blanket forming an auxiliary conductive layer on the inter-electrode dielectric; and

planarizing the top surface of stacked layer of the auxiliary conductive layer and the inter-electrode dielectric so as to expose the top surfaces of the device isolation films so that the auxiliary conductive layer can be selectively embedded in grooves defined by the steps.

12. The method of claim 11, after forming the periodic structure, further comprising:

etching sidewalls of device isolation films exposed at spaces implemented by the steps so as to widen the width of the spaces,

before blanket forming the inter-electrode dielectric.

13. The method of claim 9, wherein the forming inter-electrode dielectrics comprises:

removing natural oxide films formed on surfaces of the first conductive layers by gas etching in a CVD furnace; and

forming selectively the inter-electrode dielectrics on the top surface of the first conductive layers in the CVD furnace, keeping the natural oxide removed surface of the first conductive layers airtight.

14. The method of claim 13, wherein the forming selectively the inter-electrode dielectrics is executed at substrate temperatures between 500° C to 700° C.

15. The method of claim 13, wherein the forming selectively the inter-electrode dielectrics is executed by CVD process using silicon halide as a source gas.

16. The method of claim 15, wherein the silicon halide is a chloride compound.

17. The method of claim 16, wherein the chloride compound is a compound selected from the group consisting of tetrachlorosilane and trichlorosilane.

18. The method of claim 9, wherein the forming the periodic structure comprises:

forming the cell site gate insulator on the semiconductor substrate;

forming the first conductive layer on the cell site gate insulator;

forming an end point monitoring film on the first conductive layer, the end point monitoring film having different etching behavior from the device isolation film;

forming a masking film on the end point monitoring film, the masking film having the same etching behavior as the device isolation film;

delineating the masking film so as to form an etching mask;

selectively etching the end point monitoring film, the first conductive layer, the cell site gate insulator and an upper portion of the semiconductor substrate so as to form a plurality of device isolation grooves running along the column-direction, defining a plurality of the second ridges arranged alternatively between the device isolation grooves;

blanket forming the device isolation film so as to fill in the device isolation grooves;

planarizing the top surface of the device isolation film so as to expose periodically a plurality of the top surfaces of the end point monitoring films; and

etching selectively the end point monitoring films, employing the difference of the etching behaviors.

19. The method of claim 18, after etching selectively the end point monitoring films, further comprising:

planarizing the top surface of the device isolation film so as to expose periodically a plurality of the top surfaces of the first conductive layer; and

removing selectively the exposed top surfaces of the first conductive layers so that each of the top surfaces of the first conductive layers manifests a curved surface such that both edges of the curved surface are higher than the level of the central portion of the curved surface.

20. The method of claim 9, wherein each of the inter-electrode dielectrics is a single layer film selected from the group consisting of an silicon oxide film, a silicon nitride film, an aluminum oxide film, a hafnium oxide film and a zirconium oxide film or a composite film including at least one of the single layer film.